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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,371	12/02/2003	Kenji Suzuki	96790P445	7125

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EXAMINER
VLAHOS, SOPHIA

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/726,371	SUZUKI ET AL.	
	Examiner	Art Unit	
	SOPHIA VLAHOS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/15/2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2,3 and 5-65* is/are allowed.

6)☒ Claim(s) *1,66 and 67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 August 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/30/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings (Fig. 38, Fig. 39, Fig 40A, Fig. 40B) with the added "prior art" label were received on 8/15/2007. These drawings are acceptable.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Saito et. al., (U.S. 5,940,432).

With respect to claim 1, Saito et. al., disclose: a spreading code generating section which generates a spreading code for correlating with a received spread signal (Fig. 11, block 84 "PN code generator, PN code supplied to multiplier 821 multiplied (correlated) with reception signal, column 11, lines 5-7); a correlation value computing section which computes a correlation value between the spread signal and the spreading code output from said spreading code generating section (see Fig. 11, combination of elements 821 (multiplier), 822 (integrator), 823 (power converter), column 11, lines 5-14); a data signal demodulating section (Fig. 11, combination of blocks 81, 82, 83 corresponding to the claimed data signal demodulating section) which detects a peak of an output from said correlation value computing section and

demodulates a data signal on the basis of the detected peak (Fig. 11, elements 82, 825 that control switch 826, column 11, lines 19-23, where the detected peak corresponds to the correlation value being larger than the threshold, see column 12, lines 11-24) ; a peak signal detecting section which detects the peak of the output from said correlation value computing section (Fig. 11, element 82) and a spreading code generation control section which changes a shifting direction of the spreading code relative to the spread signal every time a peak is detected by said peak signal detecting section (see column 11, lines 61-67, through column 12, lines 1-24, shift in lag direction or leading direction of the PN code, every time clock tracking mode is perfomed) .

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 66 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et. al., (U.S. 5,940,432) in view of Hiramatsu et. al., (U.S. 5,031,191).

With respect to claim 66, Saito et. al., do not expressly teach: a filter which passes only a signal component, of a signal output from said data signal demodulating section, which falls within a data frequency band.

In the same field of endeavor (spread spectrum demodulators) Hiramatsu

et. al., disclose: a filter which passes only a signal component, of a signal which falls within a data frequency band (see Fig. 1, BPF signal 110, function of band pass filter is to pass signal which falls within a data frequency band).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Saito based on the teachings of Hiramatsu et. al., so that it includes a filter which passes only a signal component, of a signal output from said data signal demodulating section, which falls within a data frequency band, so that only a signal of interest is retained (by the BPF) and unwanted signal frequencies are filtered out.

6. Claim 67 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saito et. al., (U.S. 5,940,432) in view of Uchida et. al., (U.S. 6,366,603).

With respect to claim 67, Saito et. al., do not expressly teach: further comprising demodulation means for demodulating a data signal by counting peaks of outputs from said correlation value computing section in place of said data signal demodulating section.

In the same field of endeavor (spread spectrum communications), Uchida et. al., disclose: demodulation means for demodulating a data signal by counting peaks of outputs from said correlation value computing section (column 3, lines 9-27, see Fig. 1, blocks within dashed lines and demodulator 21 and Fig. 6 process described in column 8, lines 43-67, through column 9, lines 1-16).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Saito et. al., based on the teachings of Uchida et. al., so that it includes demodulation means for demodulating a data signal by counting peaks of outputs from said correlation value computing section in place of said data signal demodulating section, so that communication is performed by merely counting the number of correlation peaks before data demodulation, so that high speed media access is performed even under unfavorable electric-wave environment (Uchida et. al., column 3, lines 23-27)

Allowable Subject Matter

7. The following is an examiner's statement of reasons for allowance:

The prior art of the record fails to teach or suggest alone or in combination:

A spread-spectrum demodulator comprising:

a first spreading code generating circuit which generates N first spreading codes in synchronism with a second clock; a second spreading code generating circuit which generates N second spreading codes obtained by rearranging the first spreading codes in reverse order in synchronism with the second clock; a peak detector which detects a peak of an output from said adder and demodulates a data signal on the basis of the detected peak; and a spreading code control circuit which alternately switches inputting of the first spreading codes from the first spreading code generating circuit to said multipliers and inputting of the second spreading code from said second spreading code generating circuit to said multipliers every time the peak is by said peak detector, as

recited in independent claims 2, 10, 27, 29, 31 and in combination with other elements of the respective claims.

Claims 2,3, 42-44 are allowed.

Claims 10-11,45-47 are allowed.

Claims 27-28, 57-59 are allowed.

Claims 29-30, 60-62 are allowed.

Claims 31-32, 63-65 are allowed.

The prior art of the record fails to teach or suggest alone or in combination:

A spread-spectrum demodulator comprising:

A clock control circuit which controls inputting of the second clock to said spreading code generating circuit in accordance with detection of the peak by said peak detector, wherein said clock control circuit alternately switches stoppage and resumption of inputting of the second clock to said spreading code generating circuit every time the peak is detected by said peak detector, as recited in claim 5 and in combination with other elements of the claim.

Claim 5 is allowed.

The prior art of the record fails to teach or suggest alone or in combination:

A spread-spectrum demodulator comprising: a clock control circuit which controls inputting of the second clock to said spreading code generating circuit in accordance with detection of the peak by said peak detector, wherein said clock control circuit stops inputting the second clock to said spreading code generating circuit for a predetermined time when the peak is detected by said detector, as recited in claim 6 and in combination with other elements of the claim.

Claims 6 is allowed.

The prior art of the record fails to teach or suggest alone or in combination:

A spread-spectrum demodulator comprising: a first spreading code generating circuit which generates N first spreading codes in synchronism with a second clock;

a second spreading code generating circuit which generates N second spreading codes obtained by rearranging the first spreading codes in reverse order in synchronism with the second clock; a polarity conversion circuit which outputs nearly half of the N spreading codes output from said first spreading code generating circuit or said second spreading code generating circuit which correspond to either newer or older spread signals in a reception order upon performing polarity conversion such that each of the spreading codes exhibits two polarity states, i.e., inverted and noninverted states, during one period of the second clock, and outputs remaining nearly half of the codes without any change, a peak detector which detects a peak of an output from said adder and demodulates a data signal on the basis of the detected peak; and

a spreading code control circuit which alternately switches inputting of the first spreading codes from said first spreading code generating circuit to said polarity conversion circuit and inputting of the second spreading codes from said second spreading code generating circuit to said polarity conversion circuit every time the peak is detected by said peak detector, as recited in claim 12, and in combination with other elements of the claim.

Claims 12-13, 48-50 are allowed.

The prior art of the record fails to teach or suggest alone or in combination:

A spread-spectrum demodulator comprising: a first spreading code generating circuit which generates N first spreading codes in synchronism with a second clock;

a second spreading code generating circuit which generates N second spreading codes obtained by rearranging the first spreading codes in reverse order in synchronism with the second clock; a polarity conversion circuit which outputs nearly half of multiplier output signals from said N multipliers which correspond to either newer or older spread signals in a reception order upon performing polarity conversion such that each of the multiplier output signals exhibits two polarity states, i.e., inverted and noninverted states, during one period of the second clock, and outputs remaining nearly half of the multiplier output signals without any change, a peak detector which detects a peak of an output from said adder and demodulates a data signal on the basis of the detected peak; and a spreading code control circuit which alternately switches inputting of the

first spreading codes from said first spreading code generating circuit to said multipliers and inputting of the second spreading codes from said second spreading code generating circuit to said multipliers every time the peak is detected by said peak detector, as recited in claim 14 and in combination with other elements of the claim.

Claims 14-15, 51-53 are allowed.

The prior art of the record fails to teach or suggest alone or in combination:

A spread-spectrum demodulator comprising: a first spreading code generating circuit which generates N first spreading codes in synchronism with a second clock;

a second spreading code generating circuit which generates N second spreading codes obtained by rearranging the first spreading codes in reverse order in synchronism with the second clock; a polarity conversion circuit which outputs nearly half of sample/hold output signals from said N sample/hold circuits which correspond to either newer or older spread signals in a reception order upon performing polarity conversion such that each of the sample/hold output signals exhibits two polarity states, i.e., inverted and noninverted states, during one period of the second clock, and outputs remaining nearly half of the sample/hold signals without any change, N multipliers which multiply signals output from said polarity conversion circuit and spreading codes output from said first spreading code generating circuit or said second spreading code generating circuit;

a peak detector which detects a peak of an output from said adder and demodulates a data signal on the basis of the detected peak; and a spreading code control circuit

which alternately switches inputting of the first spreading codes from said first spreading code generating circuit to said multipliers and inputting of the second spreading codes from said second spreading code generating circuit to said multipliers every time the peak is detected by said peak detector, as recited in claim 16 and in combination with other elements of the claim.

Claims 16-17, 54-56 are allowed.

The prior art of the record fails to teach or suggest alone or in combination:
A spread-spectrum demodulator comprising: a polarity conversion circuit which outputs nearly half of the N spreading codes output from said spreading code generating circuit which correspond to either newer or older spread signals in a reception order upon performing polarity conversion such that each of the spreading codes exhibits two polarity states, i.e., inverted and noninverted states, during one period of the second clock, and outputs remaining nearly half of the codes without any change; as recited in claims 18, 33 and in combination with other elements of the respective claims.

Claims 18-20 are allowed.

Claims 33-35 are allowed

The prior art of the record fails to teach or suggest alone or in combination: A spread-spectrum demodulator comprising: a polarity conversion circuit which outputs nearly half of the multiplier output signals from said N multipliers which correspond to either newer

or older spread signals in a reception order upon performing polarity conversion such that each of the multiplier output signals exhibits two polarity states, i.e., inverted and noninverted states, during one period of the second clock, and outputs remaining nearly half of the multiplier output signals without any change; as recited in claims 21, 36 and in combination with other elements of the respective claims.

Claims 21-23 are allowed.

Claims 36-38 are allowed.

The prior art of the record fails to teach or suggest alone or in combination: A spread-spectrum demodulator comprising: a polarity conversion circuit which outputs nearly half of the sample/hold output signals from said N sample/hold circuits which correspond to either newer or older spread signals in a reception order upon performing polarity conversion such that each of the sample/hold output signals exhibits two polarity states, i.e., inverted and noninverted states, during one period of the second clock, and outputs remaining nearly half of the sample/hold output signals without any change; N multipliers which multiply signals output from said polarity conversion circuit and spreading codes output from said spreading code generating circuit for each corresponding signal; as recited in claims 24, 39 and in combination with other elements of the respective claims.

Claims 24-26 are allowed.

Claims 39-41 are allowed.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is 571 272 5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SV
10/26/2007

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